Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A method for providing bitline contacts in a memory cell array, which comprises:

disposing a plurality of bitlines in a first direction;

covering the bitlines with an isolating layer;

~~disposing a plurality of wordlines in a second direction~~ crossing the first direction above the bitlines;

disposing memory cells where the bitlines and wordlines cross one another;

removing the isolating layer completely from the bitlines at portions not covered by the wordlines with areas between the bitlines remaining unaffected, carrying out the step of removing the isolating layer from the bitlines by:

depositing a photoresist material;

patterning the photoresist material using a mask having a stripe pattern; and

selectively etching the isolating layer with respect to the wordlines; and

providing an electrical conductive material on exposed portions of the bitlines.

Claim 2 (cancelled).

Claim 3 (currently amended). The method according to claim [[2]] 1, which further comprises providing the mask having the stripe pattern as the bitline mask by which the bitlines have been defined.

Claim 4 (currently amended). The method according to claim [[2]] 1, which further comprises carrying out the bitline disposing step by disposing the bitlines with the mask having the stripe pattern.

Claim 5 (currently amended). A method for providing bitline contacts in a memory cell array, which comprises:

disposing a plurality of bitlines in a first direction on a substrate;

disposing a plurality of wordlines in a second direction crossing the first direction above the bitlines on the substrate;

disposing memory cells where the bitlines and wordlines cross one another, the memory cells forming a memory cell array;

covering the bitlines with a first isolating layer;

covering, with at least one second isolating layer, all portions of the memory cell array between the bitlines not covered by the wordlines;

removing the first isolating layer from the bitlines by a step in which also a topmost of the at least one second isolating layer is removed from the memory cell array at portions not covered by the wordlines, carrying out the removing step by:

depositing a phtoresist material;

photolithographically patterning the photoresist material causing the photoresist material to be removed within the

memory cell array but remain in a peripheral portion of the array; and

selectively etching each of the second and first isolation layers causing the isolation layer to be completely removed from the bitlines in areas not covered by the word lines; and

providing an electrical conductive material on exposed portions of the bitlines.

Claim 6 (original). The method according to claim 5, which further comprises carrying out the step of removing the first isolating layer by time-controlled etching of the first isolating layer selectively with respect to the wordlines.

Claim 7 (original). The method according to claim 1, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing an isolating material onto the memory cell array;

coating a photoresist material and lithographically defining contact holes in the photoresist material;

etching the isolating material to create the contact holes; and

depositing the electrical conductive material to fill the contact holes with the electrical conductive material.

Claim 8 (original). The method according to claim 5, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing an isolating material onto the memory cell array;

coating a photoresist material and lithographically defining contact holes in the photoresist material;

etching the isolating material to create the contact holes; and

depositing the electrical conductive material to fill the contact holes with the electrical conductive material.

Claim 9 (original). The method according to claim 1, which further comprises carrying out the step of providing the

electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

Claim 10 (original). The method according to claim 2, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

Claim 11 (original). The method according to claim 3, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

Claim 12 (original). The method according to claim 9, which further comprises carrying out the step of removing the electrical conductive material from the areas between the bitlines by:

coating a photoresist material on the electrical conductive material and lithographically defining regions where the electrical conductive material is to be removed using a mask having a stripe pattern; and

removing the electrical conductive material in the exposed regions.

Claim 13 (original). The method according to claim 5, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

Claim 14 (original). The method according to claim 6, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

Claim 15 (original). The method according to claim 13, which further comprises carrying out the step of removing the electrical conductive material from the areas between the bitlines by:

coating a photoresist material on the electrical conductive material and lithographically defining regions where the electrical conductive material is to be removed using a mask having a stripe pattern; and

removing the electrical conductive material in the exposed regions.

Claim 16 (original). The method according to claim 15, which further comprises carrying out the step of removing the first isolating layer from the bitlines to expose the substrate at the portions between the bitlines not covered by the wordlines, and performing the step of etching the electrical

conductive material as an over-etching step to remove part of the substrate under the electrical conductive material.

Claim 17 (original). The method according to claim 9, which further comprises carrying out the depositing an isolating material depositing step by depositing, in the areas between the bitlines, a silicate glass doped with at least one of boron and phosphorous.

Claim 18 (original). The method according to claim 13, which further comprises carrying out the depositing an isolating material depositing step by depositing, in the areas between the bitlines, a silicate glass doped with at least one of boron and phosphorous.

Claim 19 (original). The method according to claim 1, which further comprises carrying out the electrical conductive material providing step by providing doped polysilicon on exposed portions of the bitlines.

Claim 20 (original). The method according to claim 5, which further comprises carrying out the electrical conductive material providing step by providing doped polysilicon on exposed portions of the bitlines.

Claim 21 (currently amended). A method of fabricating a nitride read only memory chip, which comprises:

providing a memory cell array with memory cells, bitlines, and wordlines, each of the memory cells having a metal-insulator-semiconductor field effect transistor with the insulator being an oxide-nitride-oxide multi-layer stack for storing at least one injected electron;

disposing the bitlines in a first direction and the wordlines in a second direction perpendicular to the first direction and above the bitlines;

disposing the memory cells at points at which the bitlines and the wordlines cross one another and at which the bitlines are covered by an isolating layer;

providing a peripheral portion having logic components;

providing an electrical contact between the bitlines and metal lines to be formed in a following step by forming bitline contacts by:

removing the isolating layer completely from the bitlines at portions not covered by the wordlines with areas

between the bitlines remaining unaffected, carrying out the step of removing the isolating layer from the bitlines by:

depositing a photoresist material;

patterning the photoresist material using a mask having a stripe pattern; and

selectively etching the isolating layer with respect to the wordlines; and

providing an electrical conductive material on exposed portions of the bitlines; and

disposing the metal lines in the first direction above the bitlines.

Claim 22 (currently amended). A method of fabricating a nitride read only memory chip, which comprises:

providing a memory cell array with memory cells, bitlines, and wordlines, each of the memory cells having a metal-insulator-semiconductor field effect transistor with the insulator being

an oxide-nitride-oxide multi-layer stack for storing at least one injected electron;

disposing the bitlines in a first direction on a substrate and the wordlines in a second direction perpendicular to the first direction and above the bitlines on the substrate;

disposing the memory cells at points at which the bitlines and the wordlines cross one another and at which the bitlines are covered by a first isolating layer;

providing a peripheral portion having logic components;

providing an electrical contact between the bitlines and metal lines to be formed in a following step by forming bitline contacts by:

covering, with at least one second isolating layer, all portions of the memory cell array between the bitlines not covered by the wordlines;

removing the first isolating layer from the bitlines by a step in which also a topmost of the at least one second isolating layer is removed from the memory cell array at

portions not covered by the wordlines, carrying out the removing step by:

depositing a phtoresist material;

photolithographically patterning the photoresist material causing the photoresist material to be removed within the memory cell array but remain in a peripheral portion of the array; and

selectively etching each of the second and first isolation layers causing the isolation layer to be completely removed from the bitlines in areas not covered by the word lines; and

providing an electrical conductive material on exposed portions of the bitlines; and

disposing the metal lines in the first direction above the bitlines.

Claim 23 (original). A memory cell array having bitline contacts produced by the method according to claim 1.

Claim 24 (original). A memory cell array having bitline contacts produced by the method according to claim 5.

Claim 25 (original). A nitride read only memory chip fabricated by the method of claim 21.

Claim 26 (original). A nitride read only memory chip fabricated by the method of claim 22.